



Agilent Technologies

USB3.0 Test Report

Overall Result: PASS

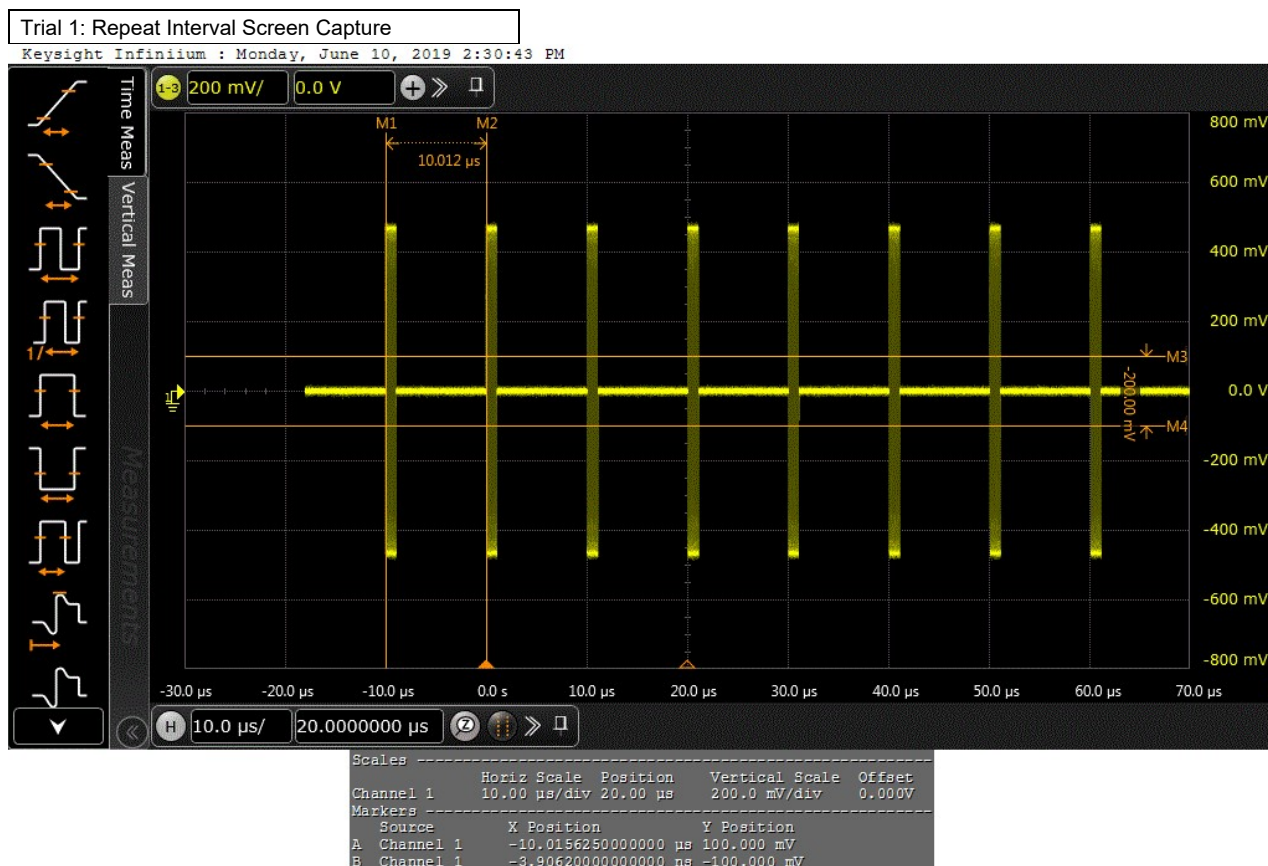
Test Configuration Details	
Device Description	
Input File Path	Device 1
Input Signal Type	Live signal
Reference Clock	SSC
De-emphasis Mode	-3.5 dB
Device	Host
Device ID:	Device 1
Test Session Details	
Infiniium SW Version	06.30.00701
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY50520122
Application SW Version	1.50
Debug Mode Used	No
Compliance Limits (official)	USB 3.0 Specification version 1.0
Probe (Channel 2)	Model: 1169A Serial: US53270102 Head: N5381A/B Atten: Calibrated (6 JUN 2019 15:46:55), Using Cal Atten (3.3595E+00) Skew: Calibrated (6 JUN 2019 15:47:04), Using Cal Skew
Probe (Channel 4)	Model: 1169A Serial: US53270106 Head: N5381A/B Atten: Calibrated (6 JUN 2019 15:48:25), Using Cal Atten (3.2294E+00) Skew: Calibrated (6 JUN 2019 15:48:36), Using Cal Skew
Last Test Date	2019-06-10 14:34:38 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	17
Total	17

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	LFPS Peak-Peak Differential Output Voltage	968.7 mV	42.2 %	800.0 mV <= VALUE <= 1.2000 V
✓	0	1	LFPS Period (tPeriod)	40.0062 ns	25.0 %	20.0000 ns <= VALUE <= 100.0000 ns
✓	0	1	LFPS Burst Width (tBurst)	1.0763 µs	40.5 %	600.0 ns <= VALUE <= 1.4000 µs
✓	0	1	LFPS Repeat Time Interval (tRepeat)	10.0186 µs	49.8 %	6.0000 µs <= VALUE <= 14.0000 µs
✓	0	1	LFPS Rise Time	276.3 ps	93.1 %	VALUE <= 4.0000 ns
✓	0	1	LFPS Fall Time	286.0 ps	92.9 %	VALUE <= 4.0000 ns
✓	0	1	LFPS Duty cycle	50.0185 %	49.9 %	40.0000 % <= VALUE <= 60.0000 %
✓	0	1	LFPS AC Common Mode Voltage	60.3 mV	39.7 %	VALUE <= 100.0 mV
✓	0	1	TSSC-Freq-Dev-Min	-4.063421 kppm	22.7 %	TSSCMin ppm <= VALUE <= TSSCMax ppm
✓	0	1	TSSC-Freq-Dev-Max	75.006 ppm	37.5 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	SSC Modulation Rate	31.080430 kHz	36.0 %	30.000000 kHz <= VALUE <= 33.000000 kHz
✓	0	1	SSC Slew Rate	4.782 ms	52.2 %	VALUE <= 10.000 ms
✓	0	1	Far End Random Jitter (CTLE ON)	171 mUI	25.7 %	VALUE <= 230 mUI
✓	0	1	Far End Maximum Deterministic Jitter (CTLE ON)	162 mUI	62.3 %	VALUE <= 430 mUI
✓	0	1	Far End Total Jitter at BER-12 (CTLE ON)	332 mUI	49.7 %	VALUE <= 660 mUI
✓	0	1	Far End Template Test (CTLE ON)	0.000	100.0 %	VALUE = 0.000
✓	0	1	Far End Differential Output Voltage (CTLE ON)	204.0 mV	9.5 %	100.0 mV <= VALUE <= 1.2000 V



✓ LFPS Rise Time

Reference: USB 3.0 Specification, Rev 1.0, Section 6.9, Table 6-20

Test Summary: Pass

Test Description: The purpose of this test is to verify that the rise time of the LFPS signal is within the conformance limits specified in Table 6-20 of the USB 3.0 Specification, version 1.0

Pass Limits: <= 4.0000 ns

Rise Time 276.3 ps

Result Details

Num Bursts Processed 5

✓ LFPS Fall Time

Reference: USB 3.0 Specification, Rev 1.0, Section 6.9, Table 6-20

Test Summary: Pass

Test Description: The purpose of this test is to verify that the fall time of the LFPS signal is within the conformance limits specified in Table 6-20 of the USB 3.0 Specification, version 1.0

Pass Limits: <= 4.0000 ns

Fall Time 286.0 ps

Result Details

Num Bursts Processed 5

✓ LFPS Duty cycle

Reference: USB 3.0 Specification, Rev 1.0, Section 6.9, Table 6-20

Test Summary: Pass

Test Description: The purpose of this test is to verify that the duty cycle of the LFPS signal is within the conformance limits specified in Table 6-20 of the USB 3.0 Specification, version 1.0

Pass Limits: [40.0000 % to 60.0000 %]

Duty cycle (%) 50.0185 %

Result Details

Num Bursts Processed 5

✓ LFPS AC Common Mode Voltage

Reference: USB 3.0 Specification, Rev 1.0, Section 6.9, Table 6-20

Test Summary: Pass

Test Description: The purpose of this test is to verify that the maximum voltage from Txp + Txn for both time and amplitude is within the limits as specified in Table 6-20 of the USB 3.0 specification

Pass Limits: ≤ 100.0 mV

AC Common Mode Voltage 60.3 mV

Result Details



TSSC-Freq-Dev-Min

Reference: USB 3.0 Specification, Rev 1.0, Section 6.5.3, Table 6-9

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured SSC deviation is within the conformance limits specified in Table 6-9 of the USB 3.0 Specification.

Pass Limits: [TSSCMin ppm to TSSCMax ppm]

SSC Deviation (ppm) -4.063421 kppm

Result Details

Max UI (ppm) -3.993984 kppm

Min UI (ppm) -4.063421 kppm

SSC Profile (See image)

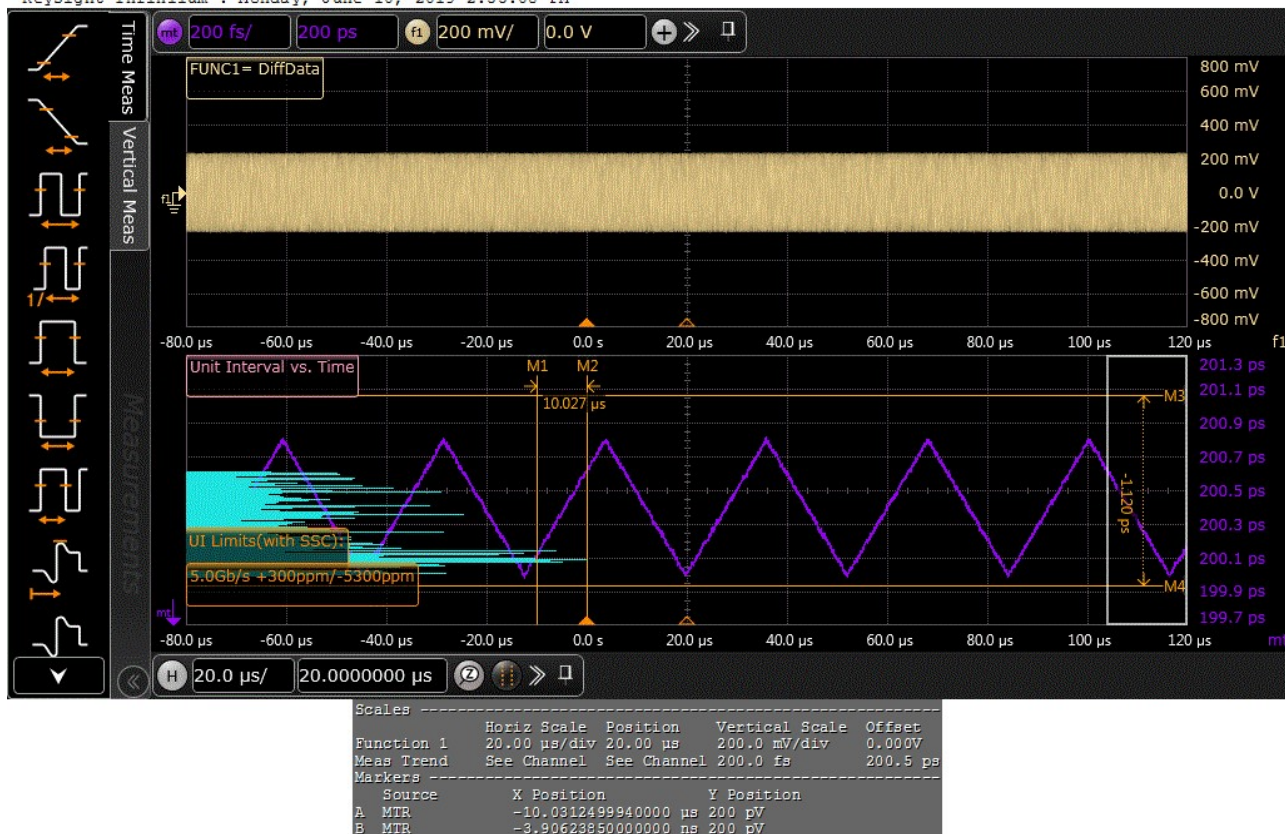
PassLimit Min (TSSCMin) -5.300000 kppm

PassLimit Max (TSSCMax) -3.700000 kppm

Trial 1

Trial 1: SSC Profile

Keysight Infiniium : Monday, June 10, 2019 2:33:08 PM



TSSC-Freq-Dev-Max

Reference: USB 3.0 Specification, Rev 1.0, Section 6.5.3, Table 6-9

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured SSC deviation is within the conformance limits specified in Table 6-9 of the USB 3.0 Specification.

Pass Limits: [-300.000 ppm to 300.000 ppm]

Worst SSC Deviation (ppm) 75.006 ppm

Result Details

Max UI (ppm) 75.006 ppm

Min UI (ppm) -5.000 ppm



SSC Modulation Rate

Reference: USB 3.0 Specification, Rev 1.0, Section 6.5.3, Table 6-9

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured SSC modulation rate is within the conformance limits specified in Table 6-9 of the USB 3.0 Specification.

Pass Limits: [30.000000 kHz to 33.000000 kHz]

Modulation Rate (Hz) 31.080430 kHz

Result Details

Modulation rate measurement Success



SSC Slew Rate

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.1, Table 6-10

Test Summary: Pass

Test Description: The purpose of this test is to ensure the combination of SSC and all other jitter sources within the bandwidth of the CDR must not exceed the allowed slew rate as listed in Table 6-10.

Pass Limits: <= 10.000 ms

Max Slew Rate 4.782 ms

Result Details

Slew Rate (See image)

Min Phase -2.33 ms

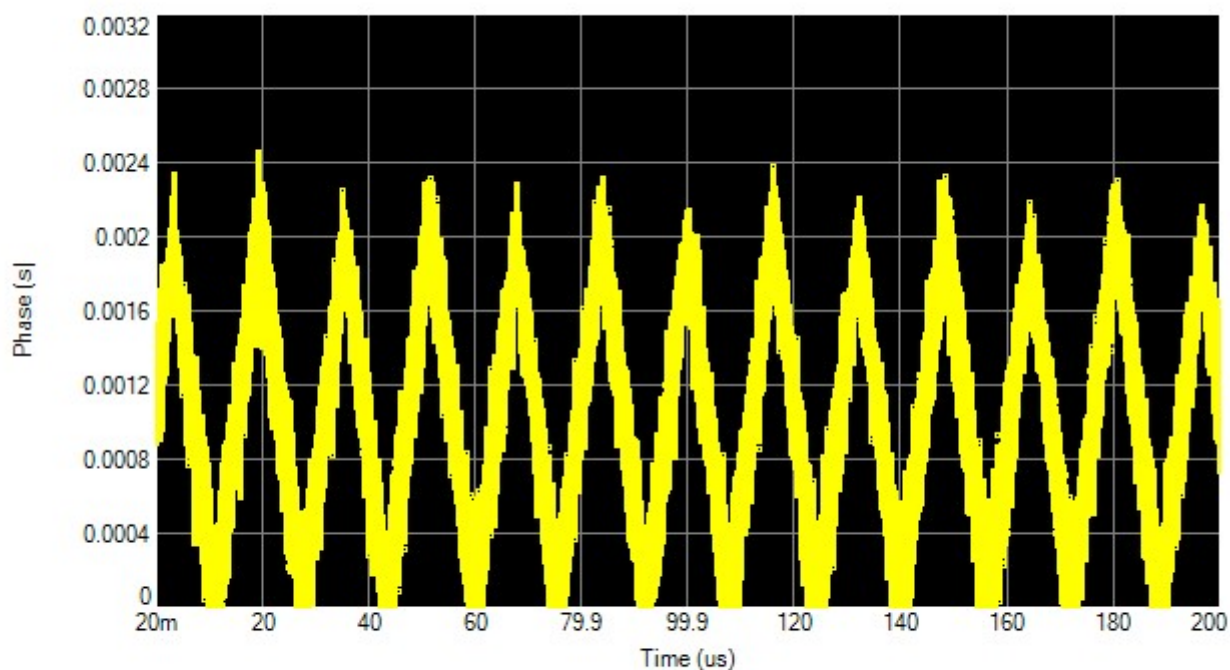
Max Phase 2.45 ms

Test Pattern CP1

Trial 1

Trial 1: Slew Rate

Phase Jitter Slew Rate



Legend:

Slew Rate



Far End Random Jitter (CTLE ON)

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.3, Table 6-12

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured random jitter, Rj measured at TP1 is within the limits as specified in Table 6-12 of the USB 3.0 specification.

Pass Limits: <= 230 mUI

RJ 171 mUI

Result Details

Total #UI Measured 1.000000000 M

Rj_rms 2.426 ps

Test Pattern CP1

De-embed Settings Normal Channel

Embedded channel file USB3_TX_Host_Channel.tf4

Test Waveform (See image)

Trial 1



Far End Maximum Deterministic Jitter (CTLE ON)

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.3, Table 6-12

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured deterministic jitter, Dj measured at TP1 is within the limits as specified in Table 6-12 of the USB 3.0 specification.

Pass Limits: ≤ 430 mUI

DJ 162 mUI

Result Details

Total #UI Measured 1.000000000 M

DJ_dd 32.349 ps

Rj_rms 2.426 ps

Test Pattern CP0

De-embed Settings Normal Channel

Embedded channel file USB3_TX_Host_Channel.tf4

Far End Total Jitter at BER-12 (CTLE ON)

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.3, Table 6-12

Test Summary: Pass

Test Description: The purpose of this test is to verify that the measured total jitter, Tj measured at TP1 is within the limits as specified in Table 6-12 of the USB 3.0 specification.

Pass Limits: ≤ 660 mUI

Tj at BER 10-12 332 mUI

Result Details

Total #UI Measured 1.000000000 M

Tj at BER 10-12 66.479 ps

Rj_rms(ps) 2.426 ps

Rj_rms(UI) 12 mUI

DJ_dd(ps) 32.349 ps

DJ_dd(UI) 162 mUI

RJ Test Pattern CP1

DJ Test Pattern CP0

TJ Equation TJ = DJ(CP0) + 14.069 * RJrms(CP1)

Far End Template Test (CTLE ON)

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.3, Table 6-12

Test Summary: Pass

Test Description: The purpose of this test is to perform an eye mask test at TP1 using the eye mask template as specified in table 6-12 of the USB 3.0 specification.

Pass Limits: = 0.000

Eye Test 0.000

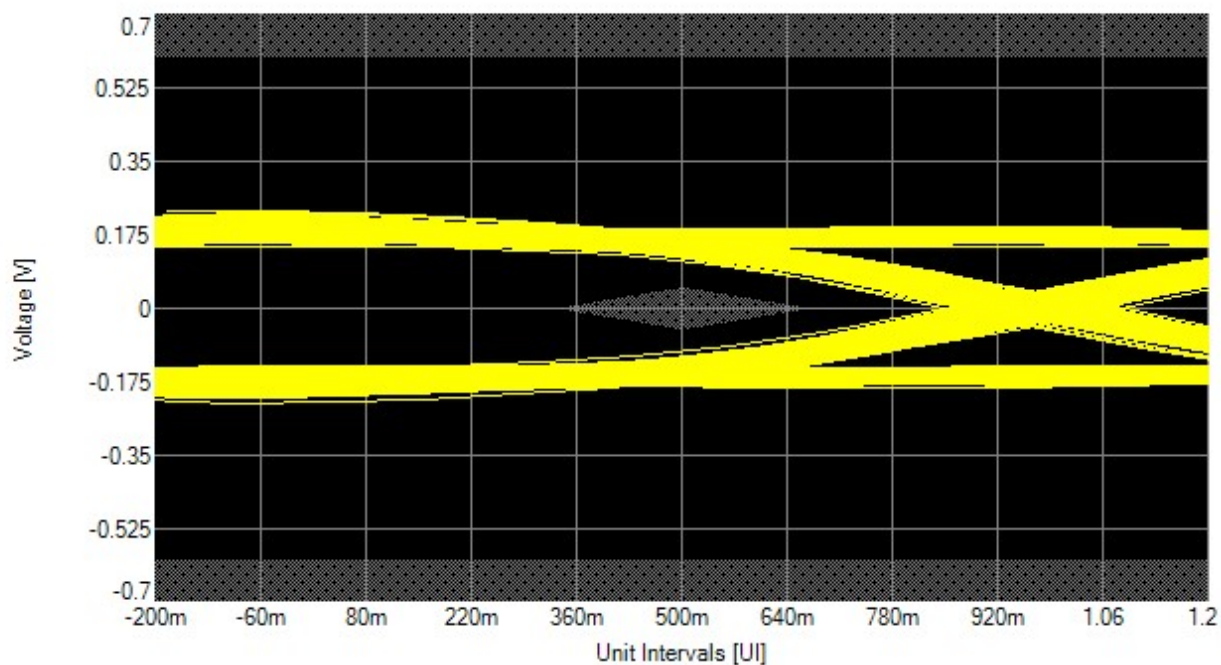
Result Details

Total #UI Measured	1.000000000 M	Non-Transition Failures	0.000	Transition Failures	0.000
Non-Transition Eye Diagram	(See image)	Transition Eye Diagram	(See image)	Total Failures	0.000
NonTrans Max Voltage	227 m	NonTrans Min Voltage	-226 m	NonTrans Lower Margin Voltage	56 m
NonTrans Upper Margin Voltage	58 m	NonTrans Eye Height	214 m	Trans Max Voltage	232 m
Trans Min Voltage	-228 m	Trans Lower Margin Voltage	50 m	Trans Upper Margin Voltage	54 m
Trans Eye Height	204 m	Test Pattern	CP0	De-embed Settings	Normal Channel
Embedded channel file	USB3_TX_Host_Channel.tf4	Pulsewidth_min_CP0	373.490 ps		
Pulsewidth_max_CP0	1.628350 ns				

Trial 1

Trial 1: Non-Transition Eye Diagram

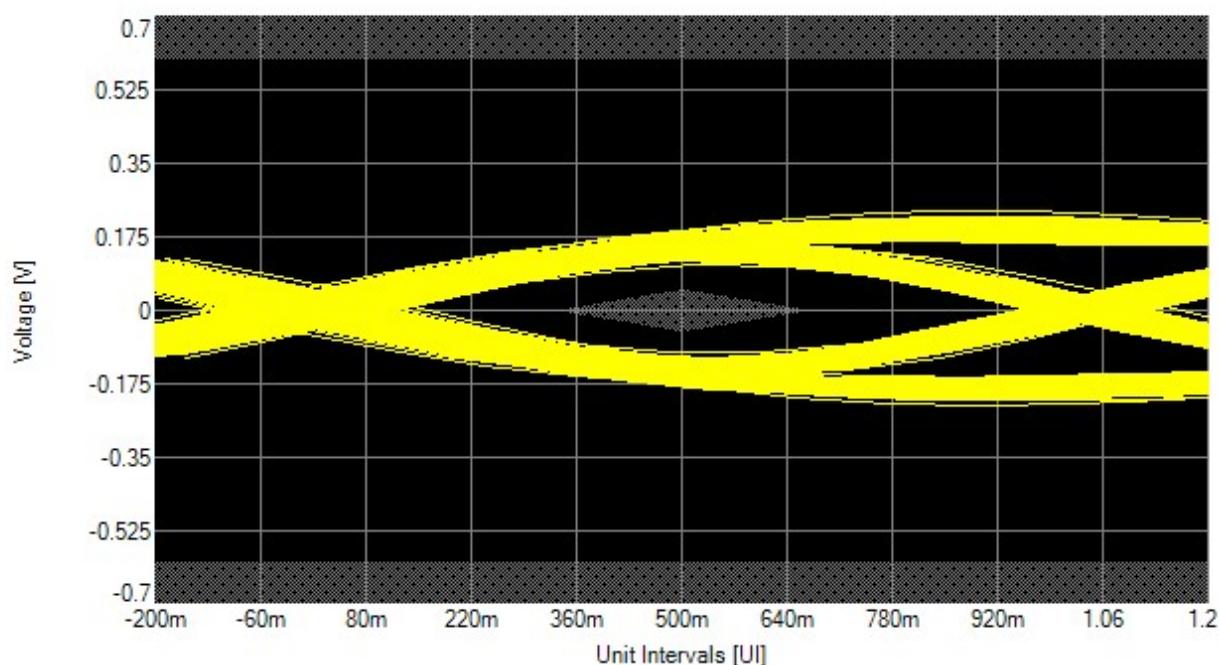
Eye Diagram



Legend:

Waveform

Trial 1: Transition Eye Diagram

Eye Diagram**Legend:**
 **Waveform**
 Far End Differential Output Voltage (CTLE ON)

Reference: USB 3.0 Specification, Rev 1.0, Section 6.7.3, Table 6-12

Test Summary: **Pass**

Test Description: The purpose of this test is to verify that the differential output voltage measured at TP1 meets the minimum eye height as specified in Table 6-12 of the USB 3.0 specification.

Pass Limits: [100.0 mV to 1.2000 V]**PeakToPeakVoltage** 204.0 mV**Result Details****Total #UI Measured** 1.000000000 M**Max. Transition Eye Height** 460.2 mV**Min. Transition Eye Height** 204.0 mV**Max. Transition Voltage** 232.3 mV**Min. Transition Voltage** -227.9 mV**Max. Transition Inner Eye Voltage** 103.7 mV**Min. Transition Inner Eye Voltage** -100.3 mV**Max. Non Transition Eye Height** 452.7 mV**Min. Non Transition Eye Height** 213.8 mV**Max. Non Transition Eye Voltage** 226.9 mV**Min. Non Transition Eye Voltage** -225.9 mV**Max. Non Transition Inner Eye Voltage** 108.2 mV**Min. Non Transition Inner Eye Voltage** -105.6 mV**Min. Transition Eye Voltage Margin Above Eye** 53.7 mV**Min. Transition Eye Voltage Margin Below Eye** 50.3 mV**Min. Non Transition Eye Voltage Margin Above Eye** 58.2 mV**Min. Non Transition Eye Voltage Margin Below Eye** 55.6 mV**Test Pattern** CP0